

09/828,862
FUS.019DIV

REMARKS

Claims 3-17 are all the claims presently pending in the application. Claims 3-5 have been amended to more particularly define the invention. Claims 8-17 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 3-5 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Iwata et al. (U.S. Patent No. 5,880,500). Claims 6-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. (U.S. Patent No. 5,880,500).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as claimed in claim 3) is directed to a method for manufacturing a semiconductor device (e.g., an n-type metal oxide semiconductor field effect transistor (NMOSFET)).

The method includes implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse channel effect to form arsenic ion implanted regions, implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, an ion-implanted region of the phosphorous ion extending an ion-implanted region of the arsenic ion and heat-treating the ion-implanted regions for activation of the arsenic ions and the phosphorous ions to form source/drain regions

Conventional methods of forming a source/drain regions in a semiconductor device

09/828,862
FUS.019DIV

(e.g., an NMOSFET) include implanting arsenic at an acceleration energy of about 50 keV in the source/drain region. However, as channel length and source/drain regions have become smaller, a reverse short channel effect has been realized in which the threshold voltage fluctuates largely for with a change in the length of the gate. Further, if the acceleration energy of implantation is lowered to eliminate this reverse short channel effect, an undesirable increase in leakage current occurs.

The claimed method, on the other hand, implants phosphorous in the arsenic implanted regions to form a phosphorous ion-implanted region (e.g., n-type source drain buffer region) that extends beyond (e.g., below) an arsenic ion-implanted region. As a result, the acceleration energy of arsenic ion implantation may be reduced without increasing a leakage current.

II. THE IWATA REFERENCE

The Examiner alleges that Iwata discloses the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Iwata.

Iwata discloses a method of forming a semiconductor device in which phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region. Further, the phosphorous and arsenic are implanted at the same implantation energy level (e.g., 10-30 keV) (Iwata at Figure 1; col. 10, line 57-col. 11, line 15).

Applicant respectfully submits that Iwata clearly does not teach or suggest a method of forming a semiconductor device which includes "implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting step, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, a phosphorous ion-implanted region extending beyond an arsenic ion-implanted region" as recite in claim 3. As noted above, this feature is important because it allows the acceleration energy of arsenic ion implantation to be reduced without increasing a leakage current.

09/828,862
FUS.019DIV

Specifically, the Application describes that arsenic has a lower coefficient of thermal diffusion than phosphorous. Therefore, it is used instead of phosphorous to form shallower source/drain junctions (Application at page 1, line 20- page 2, line 3). However, arsenic ions are typically implanted at 50 keV which causes a reverse short channel effect (i.e., threshold voltage increases with reduction in gate length) (Application at page 3, lines 4-13). This effect could be eliminated by reducing the arsenic implant energy (e.g., to 10 keV). However, such an implant energy reduction causes a decrease in the distance between an amorphous silicon/monocrystalline silicon interface and a p-n junction interface, resulting in an increase in the p-n junction leakage current (Application at page 9, line 8-page 10, line 11).

However, the inventors of the claimed invention found that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse deeper than the arsenic ions (Application at page 10, lines 19-25). Moreover, the inventors discovered that the phosphorous ions implanted into the arsenic implanted region diffused shallower than phosphorous ions implanted without a previous arsenic implantation (Application at page 11, lines 1-5).

Therefore, the inventors have discovered that by implanting phosphorous after implanting arsenic, the distance between the amorphous silicon/ monocrystalline silicon interface and a p-n junction interface can be increased. This would allow the arsenic implantation energy to be reduced to eliminate the reverse short channel effect, without causing the p-n junction leakage current to increase (Application at page 10, lines 15-22).

Clearly, Iwata does not teach or suggest these novel features. Indeed, Iwata as noted above, Iwata does not even recognize one of the discoveries made by the inventors of the claimed invention, namely that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse deeper than the arsenic ions. This is important to the claimed invention because it helps to create a buffer region beyond the source/drain main region.

On the contrary, as noted above, in the Iwata method, the phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region. Moreover, unlike the claimed method, Iwata

09/828,862
FUS.019DIV

not the same

teaches that the phosphorous and arsenic are implanted at the same implantation energy level (e.g., 10-30 keV) (Iwata at Figure 1; col. 10, line 57-col. 11, line 15).

Therefore, Iwata clearly does not teach or suggest the inventive method which includes implanting phosphorous in arsenic ion-implanted regions to form an phosphorous ion-implanted region (e.g., n-type source drain buffer region) that extends beyond (e.g., below) an arsenic ion-implanted region.

Therefore, Applicant submits that Iwata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

The Examiner objects to the specification as not disclosing features recited in claim 3. However, Applicant notes that the specification clearly discloses implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse channel effect to form arsenic ion implanted regions (Application at page 9, lines 5-7), implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting step, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion-implanted regions (Application at page 12, lines 2-11; page 11, lines 11-14), and heat-treating the ion-implanted regions for activation of the arsenic ions and the phosphorous ions to form source/drain regions (Application at page 18, line 20-page 19, line 12).

Applicant further notes that claim 3 has been amended to change “:” to “;” as suggested by the Examiner.

In view of the foregoing, Applicant submits that claims 3-17, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed

09/828,862
FUS.019DIV

below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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Phillip E. Miller
Reg. No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 8-17 have been added.

Please amend the claims to read as follows:

3. (Amended) A method for manufacturing a semiconductor device comprising [the steps of]:
 - implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse channel effect to form arsenic ion implanted regions; [:]
 - implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting [step], at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, a phosphorous ion-implanted region extending beyond said arsenic ion-implanted region; and
 - heat-treating the ion-implanted regions for activation of the arsenic ions and the phosphorous ions to form source/drain regions, [; and
 - forming an NMOSFET having the source/drain]
4. (Amended) The method as defined in claim 3, wherein n-type impurities are implanted in said substrate [the NMOSFET region] to form an n-type extension region before the arsenic and phosphorous implanting [step].
5. (Amended) The method as defined in claim 3, wherein a dosage of the arsenic ion is determined to obtain desired electrical characteristics [required] for said semiconductor device [the NMOSFET], and an acceleration energy and a dosage of the phosphorous ion are determined such that an ion-implanted region of the phosphorous ion extends beyond a bottom surface of an ion-implanted region of the arsenic ion.